Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A1**
2. **B1**
3. **Y1**
4. **A2**
5. **B2**
6. **Y2**
7. **GND**
8. **Y3**
9. **A3**
10. **B3**
11. **Y4**
12. **A4**
13. **B4**
14. **VCC**

**.063”**

**8**

**7**

**13 12 11 10 9**

**14**

**1**

**2 3 4 5 6**

**MASK**

**REF**

**T86**

**.049”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VCC or FLOAT**

**Mask Ref: T86**

**APPROVED BY: DK DIE SIZE .049” X .063” DATE: 11/22/22**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54HCT86**

**DG 10.1.2**

#### Rev B, 7/1